

# SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

SDLS175 D2536, JANUARY 1980 — REVISED MARCH 1988

- Will Not Trigger from Clear
- D-C Triggered from Active-High or Active-Low Gated Logic Inputs
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- 'LS422 Has Internal Timing Resistor

## description

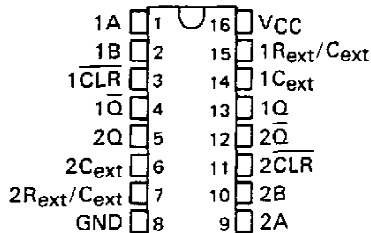
The 'LS422 and 'LS423 are identical to 'LS122 and 'LS123 except they cannot be triggered via clear.

These d-c triggered multivibrators feature output-pulse-width control by three methods. The basic pulse time is programmed by selection of external resistance and capacitance values (see typical application data). The 'LS422 contains an internal timing resistor that allows the circuits to be used with only an external capacitor, if so desired. Once triggered, the basic pulse width may be extended by retriggering the gated low-level-active (A) or high-level-active (B) inputs, or be reduced by use of the overriding clear. Figure 1 illustrates pulse control by retriggering and early clear.

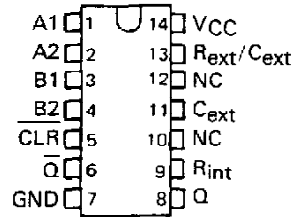
The 'LS422 and 'LS423 have enough Schmitt hysteresis to ensure jitter-free triggering from the B input with transition rates as slow as 0.1 millivolt per nanosecond. The 'LS422  $R_{int}$  is nominally 10 k ohms.

The SN54LS422 and SN54LS423 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS422 and SN74LS423 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

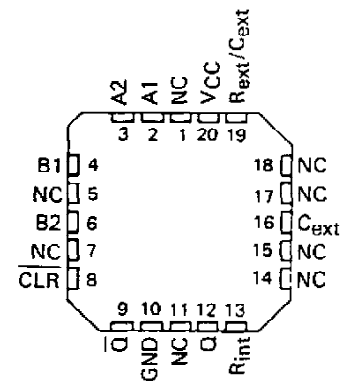
SN54LS423 . . . J OR W PACKAGE  
SN74LS423 . . . D OR N PACKAGE  
(TOP VIEW) (SEE NOTES 1 THRU 4)



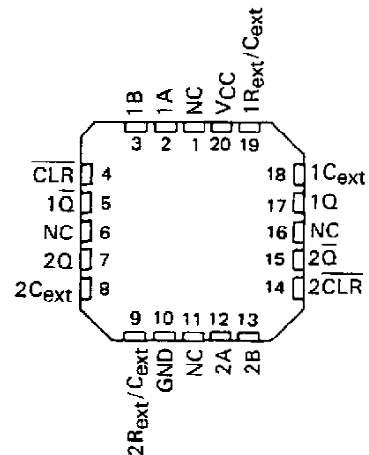
SN54LS422 . . . J OR W PACKAGE  
SN74LS422 . . . D OR N PACKAGE  
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS422 . . . FK PACKAGE  
(TOP VIEW) (SEE NOTES 1 THRU 4)



SN54LS423 . . . FK PACKAGE  
(TOP VIEW) (SEE NOTES 1 THRU 4)



- NOTES: 1. An external timing capacitor may be connected between  $C_{ext}$  and  $R_{ext}/C_{ext}$  (positive).  
 2. To use the internal timing resistor of 'LS422, connect  $R_{int}$  to  $V_{CC}$ .  
 3. For improved pulse width accuracy and repeatability, connect an external resistor between  $R_{ext}/C_{ext}$  and  $V_{CC}$  with  $R_{int}$  open-circuited.  
 4. To obtain variable pulse widths, connect an external variable resistance between  $R_{int}$  or  $R_{ext}/C_{ext}$  and  $V_{CC}$ .

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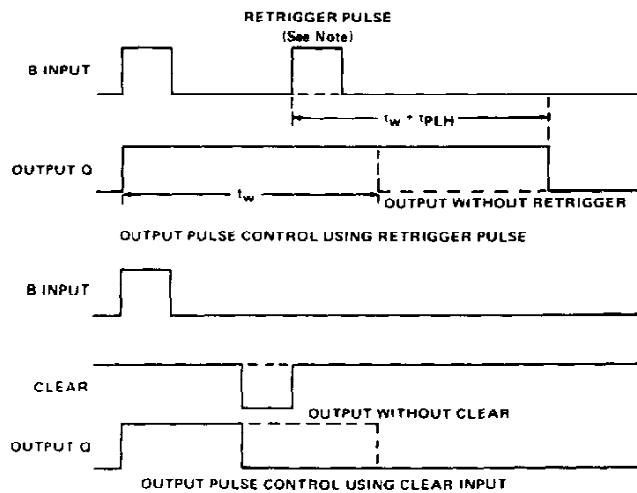
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description (continued)

LS422 FUNCTION TABLE							LS423 FUNCTION TABLE					
INPUTS						OUTPUTS		INPUTS			OUTPUTS	
CLEAR	A1	A2	B1	B2	Q	$\bar{Q}$	CLEAR	A	B	Q	$\bar{Q}$	
L	X	X	X	X	L	H	L	X	X	L	H	
X	H	H	X	X	L↑	H↑	X	H	X	L↑	H↑	
X	X	X	L	X	L↑	H↑	X	X	L	L↑	H↑	
X	X	X	X	L	L↑	H↑	H	L	↑	↓	↑	
H	L	X	↑	H	↓	↑	H	X	L	↑	H	
H	L	X	H	↑	↓	↑	H	X	L	H	↑	
H	X	L	↑	H	↓	↑	X	H	↓	H	H	
H	X	L	H	↑	↓	↑	X	↓	↓	H	H	
H	↓	↓	H	H	↓	↑	H	↓	H	H	H	
H	↓	H	H	H	↓	↑	H	↓	H	H	H	

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

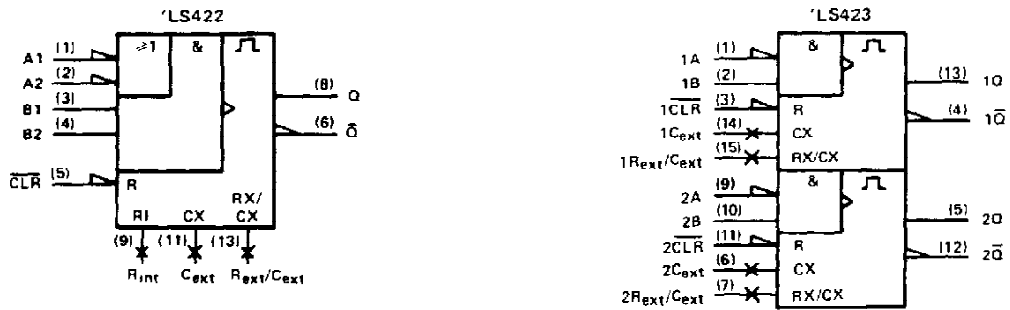


NOTE: Retrigger pulses starting before  $0.22 C_{ext}$  (in picofrads) nanoseconds after the initial trigger pulse will be ignored and the output pulse will remain unchanged.

FIGURE 1—TYPICAL INPUT/OUTPUT PULSES

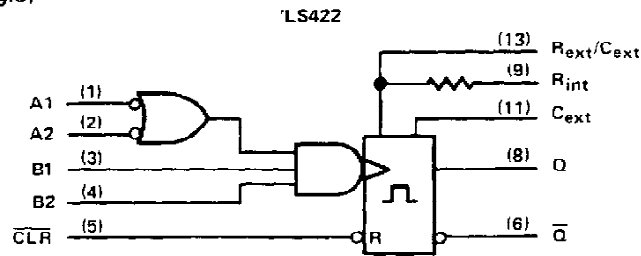
# SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

## logic symbols†

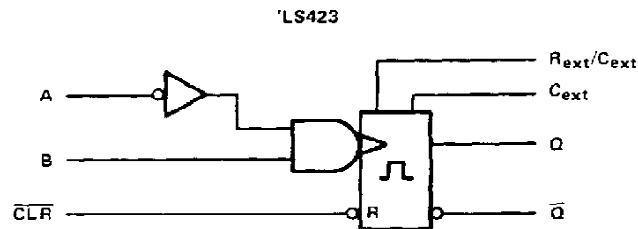


† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagrams (positive logic)

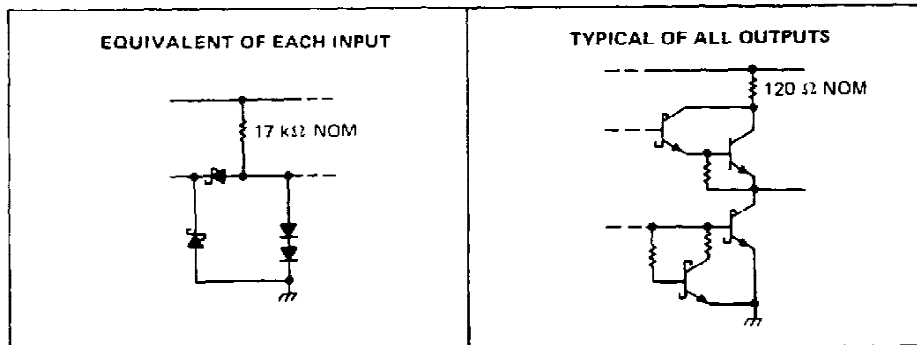


$R_{int}$  is nominally 10 k ohms



Pin numbers shown are for D, J, N, and W packages.

## schematics of inputs and outputs



# SN54LS422, SN54LS423, SN74LS422, SN74LS423 RETRIGGERABLE MONOSTABLE MULTIVIBRATORS

## recommended operating conditions

	SN54LS*			SN74LS*			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, $V_{CC}$	4.5	5	5.5	4.75	5	5.25	V
High-level output current, $I_{OH}$			-400			-400	$\mu$ A
Low-level output current, $I_{OL}$			4			8	mA
Pulse width, $t_W$	40			40			ns
External timing resistance, $R_{ext}$	5		180	5		260	k $\Omega$
External capacitance, $C_{ext}$	No restriction			No restriction			
Wiring capacitance at $R_{ext}/C_{ext}$ terminal				50			pF
Operating free-air temperature, $T_A$	-55		125	0		70	$^{\circ}$ C

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS*			SN74LS*			UNIT	
		MIN	TYP‡	MAX	MIN	TYP‡	MAX		
$V_{IH}$ High-level input voltage		2			2			V	
$V_{IL}$ Low-level input voltage				0.7			0.8	V	
$V_{IK}$ Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V	
$V_{OH}$ High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = 400 \mu\text{A}$	2.5	3.5		2.7	3.5		V	
$V_{OL}$ Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$			0.25	0.4		0.25	0.4	V
							0.35	0.5	
$I_I$ Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA	
$I_{IH}$ High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	$\mu$ A	
$I_{IL}$ Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA	
$I_{OS}$ Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA	
$I_{CC}$ Supply current (quiescent or triggered)	$V_{CC} = \text{MAX},$ See Note 6			6	11		6	11	mA
				12	20		12	20	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ .

§ Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 5. To measure  $V_{OH}$  at Q,  $V_{OL}$  at  $\bar{Q}$ , or  $I_{OS}$  at Q, ground  $R_{ext}/C_{ext}$ , apply 2 V to B and clear, and pulse A from 2 V to 0 V.  
6. With all outputs open and 4.5 V applied to all data and clear inputs,  $I_{CC}$  is measured after a momentary ground, then 4.5 V, is applied to clock.

## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$ , see note 7

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}$	A	Q	$C_{ext} = 0, R_{ext} = 5 \text{ k}\Omega, C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega$		23	33	ns
	B	Q			23	44	
$t_{PHL}$	A	$\bar{Q}$			32	45	ns
	B	$\bar{Q}$			34	56	
$t_{PHL}$	Clear	Q			20	27	ns
$t_{PLH}$	Clear	$\bar{Q}$			28	45	ns
$t_{wQ}(\text{min})$	A or B	Q		116	200	ns	
$t_{wQ}$	A or B	Q	$C_{ext} = 1000 \text{ pF}, C_L = 15 \text{ pF}, R_{ext} = 10 \text{ k}\Omega, R_L = 2 \text{ k}\Omega$	4	4.5	5	$\mu$ s

¶  $t_{wQ}$  = width of pulse output Q.

NOTE 7: Load circuits and voltage waveforms are shown in Section 1.

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## TYPICAL APPLICATION DATA FOR 'LS422, 'LS423†

The basic output pulse width is essentially determined by the values of external capacitance and timing resistance. For pulse widths when  $C_{ext} \leq 1000$  pF, use Figure 3. For  $C_{ext}$  between 0.1 nF and 1  $\mu$ F, the pulse width may be defined as:

$$t_w \approx K \cdot R_T \cdot C_{ext}$$

with K obtained from Figure 4.

When  $C_{ext} \geq 1$   $\mu$ F, the output pulse width is defined as:

$$t_w \approx 0.33 \cdot R_T \cdot C_{ext}$$

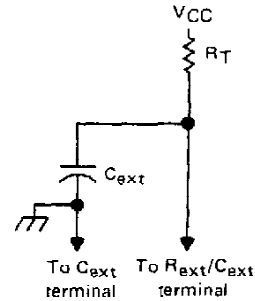
Where

$R_T$  is in kilohms (internal or external timing resistance)

$C_{ext}$  is in pF

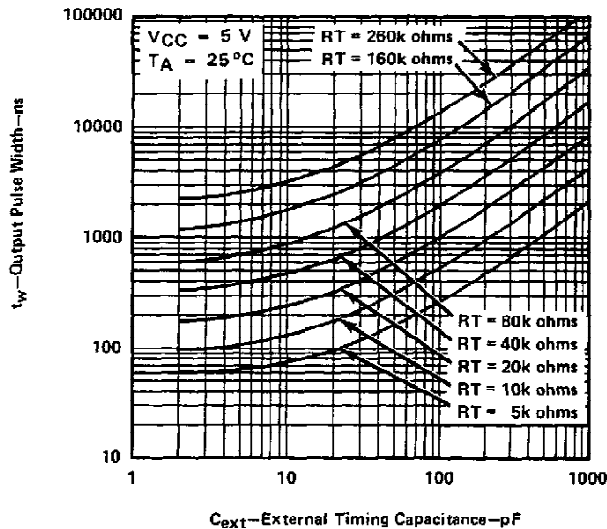
$t_w$  is in nanoseconds

For maximum noise immunity, system ground should be applied to the  $C_{ext}$  node, even though the  $C_{ext}$  node is already tied to the ground lead internally. Due to the timing scheme used by the 'LS422 and 'LS423, a switching diode is not required to prevent reverse biasing when using electrolytic capacitors.



TIMING COMPONENT CONNECTIONS  
FIGURE 2

### 'LS422, 'LS423 TYPICAL OUTPUT PULSE WIDTH vs EXTERNAL TIMING CAPACITANCE



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

FIGURE 3

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## TYPICAL APPLICATION DATA FOR 'LS422, 'LS423 †

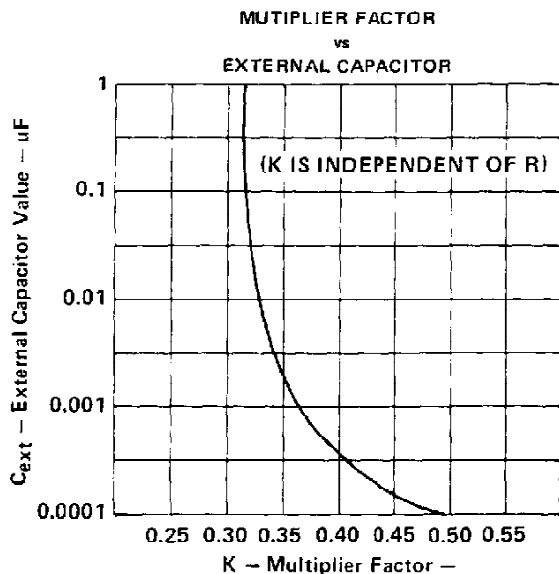


FIGURE 4

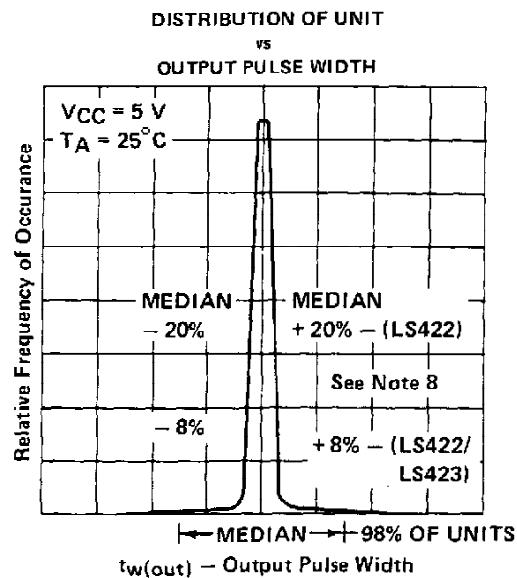


FIGURE 5

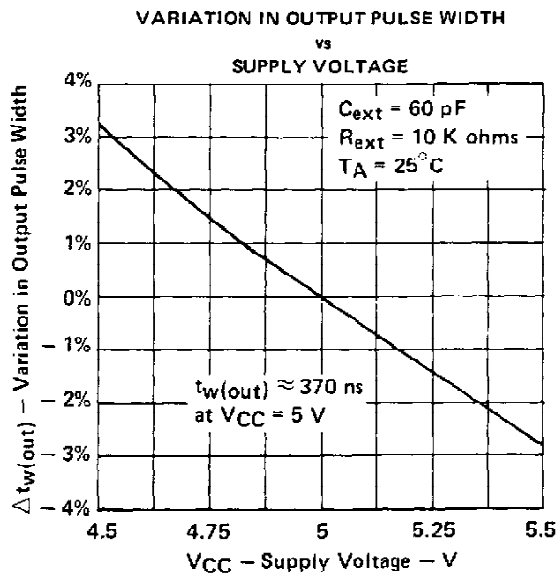


FIGURE 6

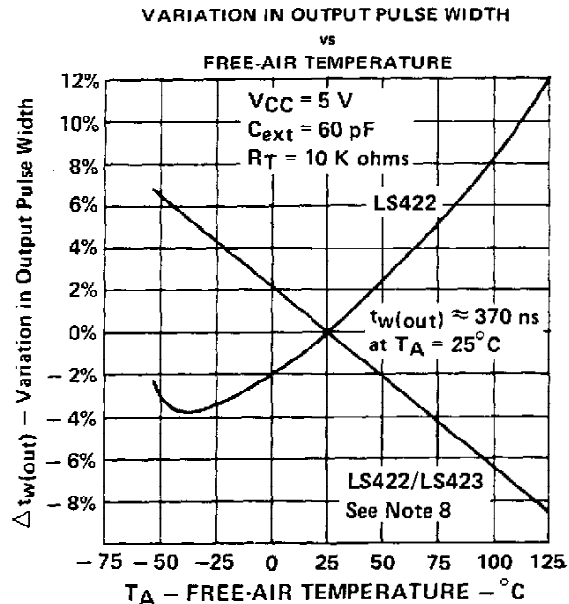


FIGURE 7

NOTE 8: For the LS422, the internal timing resistor,  $R_{int}$  was used. For the LS422/423, an external timing resistor was used for  $R_T$ .  
† Data for temperatures below  $0^\circ C$  and above  $70^\circ C$  and for supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS422 and SN54LS423 only.

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**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS423DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LS423NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS423DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74LS423NSR	SO	NS	16	2000	346.0	346.0	33.0

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